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EXAMINER	
DENNISON, JERRY B	
ART UNIT	**PAPER NUMBER**
2143	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/696,836	VANHOOF ET AL.	
	Examiner	Art Unit	
	J. Bret Dennison	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-52, 54-67, 69, 71, and 73-75* is/are rejected.

7)☒ Claim(s) *53,68,70,72 and 76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Preliminary Amendment for Application Number 09/696836 received on 25 October 2000.

2. Claims 41-76 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 21-30 recite the limitation "The method of Claim 15" in pages 93-94.

4. Claims 31,33, and 34 recite the limitation "The method of Claim 16" in page 94.

5. Claims 32 and 36 recites the limitation "The method of Claim 25" in page 94.

6. Claim 35 recites the limitation "The method of Claim 17" in page 94.

7. Claim 37 recites the limitation "The method of Claim 18" in page 94.

8. Claim 39 recites the limitation "The method of Claim 18" in page 95.

9. There is insufficient antecedent basis for this limitation in these claims.

Double Patenting (35 USC 101 Statutory)

10. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101, which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to

identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3.1 **Claim 41** is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6,212,566. This is a double patenting rejection.

U.S. Patent No. 6,212,566	***Instant Application: 09/696,836***
1. A method for defining a system specification for a digital system, said method comprising the steps of:	*41. A method for defining a system specification for a digital system, said method comprising the steps of:*
partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;	*partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;*
defining separately from said processes a data communication protocol for communication between said processes;	*defining separately from said processes a single data independent data communication protocol for communication within said digital system and between said processes;*
configuring data communication interfaces in the form of communication input ports and communication output ports for each of the processes, the communication ports forming memoryless communication channels	*configuring data communication interfaces in the form of communication input ports and communication output ports for each of tile processes, the communication ports forming memory free communication channels; and*
combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.	*combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.*

3.2 **Claim 54** is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 2 of prior U.S. Patent No. 6,212,566. This is a double patenting rejection.

U.S. Patent No. 6,212,566	***Instant Application: 09/696,836***
2. A method of implementing a digital system comprising the steps of:	*54. A method of implementing a digital system comprising the steps of:*
partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;	*partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;*
defining separately from said processes, a data communication protocol for communication between said processes;	*defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;*
organizing said data communication protocol with input and output ports for said processes, said ports using memoryless communication channels and	*organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels; and*
designing processors to implement said process	*designing a plurality of processors to implement said process.*

Double Patenting (Obviousness)

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4.1 **Claims 41, 44, 52, and 53** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,212,566. Although the conflicting claims are not identical, they are not patentably distinct from each other because.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

U.S. Patent No. 6,212,566	***Instant Application: 09/696,836***
1. A method for defining a system specification for a digital system, said method comprising the steps of:	*41. A method for defining a system specification for a digital system, said method comprising the steps of:*
partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;	*partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;*
defining separately from said processes a data communication protocol for	*defining separately from said processes a single data independent data*

communication between said processes;	*communication protocol for communication within said digital system and between said processes;*
configuring data communication interfaces in the form of communication input ports and communication output ports for each of the processes, the communication ports forming memoryless communication channels and	*configuring data communication interfaces in the form of communication input ports and communication output ports for each of tile processes, the communication ports forming memory free communication channels; and*
providing unidirectional, point-to-point connections between input ports of a first process and output ports of a second process, said input ports and said output ports being part of the associated processes,	*44. The method of claim 41, wherein said step of configuring data communication interfaces involves defining communication interfaces with the input ports and output ports to provide unidirectional, point-to-point connections between input ports of a first process and output ports of a second process, said input ports and said output ports being part of the associated processes.*
said processes implemented in C, Silage or VHDL language; and	*52. The method of Claim 44, wherein said processes arc implemented in a hardware description language or in a programming language.* *53.The method of Claim 52, wherein said processes are implemented in C, Silage or VHDL language.*
combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.	*(41) combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.*

Claims 41, 44, 52, and 53 of the application are generic to the species of invention covered by claim 1 of the patent. In that, the generic invention is "anticipated" by the species of the patented invention. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993). Thus, since anticipation is the epitome of obviousness, the claim of instant application 09/696,836 is obvious over the claim of U.S. Patent No. 6,212,566.

4.2 **Claims 54, 57, 67, and 68** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,212,566. Although the conflicting claims are not identical, they are not patentably distinct from each other because.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

U.S. Patent No. 6,212,566	***Instant Application: 09/696,836***
2. A method of implementing a digital system comprising the steps of:	*54. A method of implementing a digital system comprising the steps of:*
partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;	*partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;*
defining separately from said processes, a data communication protocol for communication between said processes;	*defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;*
organizing said data communication protocol with input and output ports for said processes, said ports using memoryless communication channels and	*organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels; and*
wherein said communication ports connect processes defined of at least one of a plurality of specifications	*67. The method of Claim 55,* wherein said communication ports connect processes defined of at least one of a plurality of specifications.
selected from a group consisting of Silage descriptions, C descriptions, VHDL process descriptions; and	*68. The method of Claim 67, wherein said plurality of specifications are* selected from a group consisting of Silage descriptions, C descriptions, VHDL process descriptions
designing processors to implement said process	*(54) designing a plurality of processors to implement said process.*
by specifying a programmable digital signal processor having a specification which conform to the processes implemented.	*57. The method of Claim 55, wherein said processor comprises a programmable digital signal processor.*

Claims 54, 57, 67, and 68 of the application are generic to the species of invention covered by claim 2 of the patent. In that, the generic invention is "anticipated" by the species of the patented invention. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993). Thus, since anticipation is the epitome of obviousness, the claim of instant application 09/696,836 is obvious over the claim of U.S. Patent No. 6,212,566.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 41-52, 54-67, 69, 71, and 73-75 are rejected under 35 U.S.C. 102(e) as being anticipated by Hansen et al. (U.S. Patent Number 5,742,840).

13. Regarding claims 41 and 54, Hansen discloses a method for defining a system specification for a digital system, said method comprising the steps of:

partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread (col. 3, lines 4-24, lines 41-43; col. 11, lines 19-41; Hansen teaches the general purpose

media processor is partitionable to handle various types of media streams using multiple threads);

defining separately from said processes a single data independent data communication protocol for communication within said digital system and between said processes (col. 3, lines 4-24, lines 41-43; Hansen teaches a single instruction stream unifies various protocols for multimedia, graphics, security and network operations);

configuring data communication interfaces in the form of communication input ports and communication output ports for each of tile processes, the communication ports forming memory free communication channels (col. 2, lines 1-6, col. 3, lines 41-43, col. 5, lines 1-19; Hansen teaches the high bandwidth interface contains the required input/output, I/O to support interprocessor communications with external devices while using system protocols and accommodating sufficient signal space to minimize channel memory effects such as noise and echo); and

defining the system includes combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification (The above steps combined define the system specifications).

14. Regarding claims 55 and 67, Hansen discloses the features of the invention, substantially as claimed, as described in claim 54, including wherein said step of designing processors comprises the step of specifying a processor having specification which conform to the processes implemented (col. 5, lines 10-22, col. 13, lines 1-20. Hansen teaches that as many as 255 separate operations are capable of being

implemented in the general purpose media processors. A microfiche appendix contains instruction sets, which can be loaded for processing, TABLE 1, These instruction sets are communicated to other processor ports across channels and links.)

15. Regarding claims 56, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said processor comprises a programmable, general purpose processor (see ABSTRACT, Hansen teaches wherein the processor comprises a programmable, general purpose processor).

16. Regarding claim 57, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said processor comprises a programmable digital signal processor (col. 1, lines 27-36, Hansen teaches digital signal processors are required to process multimedia data at faster rates than have been achieved in the prior art, Figs 3-4, col. 10, lines 24-64, Specialized processors transmit data streams at higher data rates).

17. Regarding claim 58, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said processor comprises a dedicated, custom processor (col. 10, line 65 through col. 11, line 18, Hansen teaches the general purpose media processor operates as a specialized processor, handling

audio, video, graphics and network information simultaneously, therefore making more efficient use of processor resources.).

18. Regarding claim 59, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said processor comprises custom logic circuitry with a controller such that the resulting digital system operates according to functional and realtime specifications (col. 4, line 62 through col. 5, line 9, col. 13, line 11 through col. 15, line 5, Figs9a-c, Hansen teaches the memory controllers in the high bandwidth interface transmit and receive media data formatted according to the needs of the user).

19. Regarding claim 60, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said ports and communication channels are implemented as shared memory (col. 3, lines 14-24, col. 11, lines 19-41, FIG. 6, Hansen teaches the general purpose media processor implements shared memory and I/O to communicate throughout the network).

20. Regarding claim 61, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said ports and communication channels are implemented as sockets (col. 25, lines 49-64, col. 26, lines 17-36, Hansen teaches in a distributed computing environment, transport protocols link remote processes, or sockets, with local operations. Processor ports and communication channels establish data paths to the general purpose media processors).

21. Regarding claim 62, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said ports and communication channels are implemented as files (see ABSTRACT, col. 3, lines 4-7, col. 4, lines 10-41, col. 12, line56 through col. 13, line 10, Hansen teaches a general purpose register file contains switching and math instructions for media data in its data path. These register files are configurable to transmit and receive data from any path, and are therefore programmable for all ports and channels).

22. Regarding claim 63, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said ports and communication channels are implemented as a mailbox (col. 15, line 66- through col. 16, line 31, Hansen teaches the general purpose media processor contains a memory management unit which uses cache memory to translate global virtual addresses into physical addresses, Figs 10a-b, These addresses are used to transport data across ports and channels throughout the distributed computing environment).

23. Regarding claims 64-66, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said ports and communication channels are implemented in the operating system of a multi-process operating system (col. 25, lines 49-64) for simulating the system processes and communication channels on a network of computers (col. 3, lines 52-54, Hansen teaches a system daemon uses software to replicate portions of the general purpose

media processor to other processors throughout the network environment for the execution of distributed processes, Figs 18a-c, Daemons coordinate memory access and address other processor ports through communication channels and links) and in a multi-tasking implementation shell or requester-responder (col. 25, line 65 through col. 26, line 49, Hansen teaches requester and responder daemons communicate directly with the operating systems of other processors to coordinate operations).

24. Regarding claim 69, Hansen discloses the features of the invention, substantially as claimed, as described in claim 55, including wherein said communication channels are implemented as memory mapped I/0 (col. 21, lines 25-63, Hansen teaches the general purpose media processor contains three I/O channels which organize data into packets from a memory space, once addressed, the data path determines the communication channel to pass the data).

25. Regarding claims 71, 73, and 74, Hansen discloses the features of the invention, substantially as claimed, as described in claim 56, including wherein said communication channels are implemented in integrated circuit form for communications between a first processor and a second processor across a channel, the first and second processors selected from one or more of a plurality of processor types (col. 25, lines 48-64, col. 26, lines 50-63, Hansen teaches interprocessor operations between different processors can be implemented on one or more integrated circuit chips, Fig 19.

Daemons coordinate these operations using system hardware such as another processor or a switch).

26. Regarding claim 75, Hansen discloses the features of the invention, substantially as claimed, as described in claim 57, including wherein said step of partitioning involves defining a library of auxiliary processes to simulate the digital system, the library of processes selected from a plurality of processes (col. 15, lines 55-65, Hansen teaches partitioning of processor must accommodate a variety of floating point operations using data of different bit-widths, these operations defined in software libraries).

27. Claims 53, 68, 70, 72, and 76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Hansen does not disclose the method of claim 53 wherein the communication channels are implemented as interrupt driven I/O. Hansen also does not disclose cathedral-III, ARM, VHDL processors, or an FFT process.

28. Claims 21-40 and 42-52 are method claims which correlate to rejected claims 54-67, 69, 71, and 73-75 and are rejected on the same basis.

Response to Arguments

29. Applicant's arguments filed 25 October 2000 have been fully considered but they are not persuasive.

In the remark, Applicant argued in substance that

(A) Applicant argues that, Hansen "emphasizes the use of a unified processor and teaches against heterogeneous combinations of processors" and that the method of the claims offers a way to connect different parts – subsystems or processors- defining large and complex systems being heterogeneous in nature (Applicant's paper, page 10-11).

As to point (A), in response to applicant's argument that the references fail to show certain features of the applicant's invention, it is noted that the features upon which applicant relies (i.e. heterogeneous combinations of processors) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

(B) Applicant argues that in Hansen "if one considers the general purpose media processor to be the digital system, it is evident that the communication is of different nature. Applicant also argues that if one considers the general purpose media processor and the external devices as the processes and/or processors, it is evident that the partitioning one of such processors is meant" (Applicant's paper, page 11).

As to point (B), if one considers the general purpose media processor and the external devices to be the digital system, the digital system itself is partitioned.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Bret Dennison whose telephone number is (703)305-8756. The examiner can normally be reached on M-F 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on (703)308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Bret Dennison
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